

Coder/decoder with an optical programmable logic cell

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ABSTRACT

A major research area is the representation of knowledge for a given application in a compact manner such that desired information relating to this knowledge is easily recoverable. A complicated procedure may be required to recover the information from the stored representation and convert it back to usable form. Coder/decoder are the devices dedicated to that task. In this paper the capabilities that an Optical Programmable Logic Cell offers as a basic building block for coding and decoding are analyzed.

We have previously published an Optically Programmable Logic Cells (OPLC), for applications as a chaotic generator or as basic element for optical computing. In optical computing previous studies these cells have been analyzed as full-adder units, being this element a basic component for the arithmetic logic structure in computing. Another application of this unit is reported in this paper. Coder and decoder are basic elements in computers, for example, in connections between processors and memory addressing. Moreover, another main application is the generation of signals for machine controlling from a certain instruction.

In this paper we describe the way to obtain a coder/decoder with the OPLC and which type of applications may be the best suitable for this type of cell.

Keywords: coder/decoder, line coding, code formats.

1. INTRODUCTION

In a practical communication system, the transmitter and receiver can be further broken down into many smaller blocks. For example, a transmitter may consist of blocks performing source coding, channel coding, modulation, and signal amplification. And a receiver may include blocks performing equalization, retiming, detection, demodulation, and decoding. Some of these blocks are illustrated in Fig. 1. Source coding is frequently used to reduce the number of bits in transmission. Because source coding is liable to transmission errors, channel coding is often used to detect and correct error bits by adding extra parity check bits or redundant bits. In addition, line coding is used to achieve certain properties in the transmission waveform, such as dc balance and sufficient transitions.

Line coding is also called modulation codes in a digital transmission. In digital transmissions, a bit clock must be used to sample the received signal. Because the clock should be locked in both phase and frequency, the clock must be derived from the received signal. This clock derivation is called bit-timing recovery. To facilitate this fact, bit timing must be encoded into the transmitted bits. This means a frequent signal level transition, at least every few bits, is needed.

Most of the technologies employed nowadays to implement the above facts are based on conventional systems and configurations. Although the main emphasis in the system is given to optical aspects of the structure, the way to perform line coding is based on technologies similar to those employed in electronic systems. The present paper will adopt a different approach. This approach will be based on the use of optical logic circuits, similar to those employed in optical computing and in photonic switching. The main advantage of this approach is the possibility to adopt a large variety of configurations with a larger number of applications. Namely, present line coding, as it will be shown in the first part of this paper, admits different types a codes each one with different properties and, as a consequence, with different applications. The advantage of our approach is the possibility to change the employed coding without the need to change any one of the basic components. Just a change in the signal applied to one of the control gates in the optical logic cell will permit the change to a different coding.

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Our paper will be divided into two fundamental parts. In the first one we will present a small panoramic of the main concepts in line coding. In the second one, after a short review of the properties of our optical logic cell, previously published by us in several places¹⁻⁴, we will apply its structure to the generation of a whole family of line coding. Finally, we will present some experimental results.

2. GENERAL CODER/DECODER NEEDS

There are two particular forms of data transmission that are quite common in optical communications owing to the fact that their modulation formats occur naturally in both direct and externally modulated optical sources. These two formats are referred to as non-return-to-zero (NRZ) and return-to-zero (RZ). In addition to NRZ and RZ data formats, pulse-code-modulation data signals are transmitted in other codes that are designed to optimize the link performance⁵⁻⁷.

Related with these facts line coding provides an efficient way to design an optical link. Any decision circuitry at the receiver must be able to extract precise time information from the incoming signal. This timing allow the signal to be sampled by the receiver at the time the signal-to-noise ratio is a maximum, maintains the proper pulse spacing and indicate the start and the send of each timing interval. These features are incorporated into the data stream by encoding the signal. Introducing extra bits into the raw data stream at the transmitter on a regular and logical basis and extracting them again at the receiver do this. Signal encoding gives a set of rules for arranging the signal symbols in a particular pattern. This method is called line coding. We will show in this paragraph some types of line codes employed in digital transmission on an optical link. Moreover, we will limit our discussion to binary codes because they are the more advantageous codes for this task. Another point that needs to be considered here is that the larger bandwidth needed with the new extra bits result in larger noise contributions. This factor will no be considered here because a tradeoff must be made between timing and noise bandwidth and here we will restrict ourselves to the timing aspect.

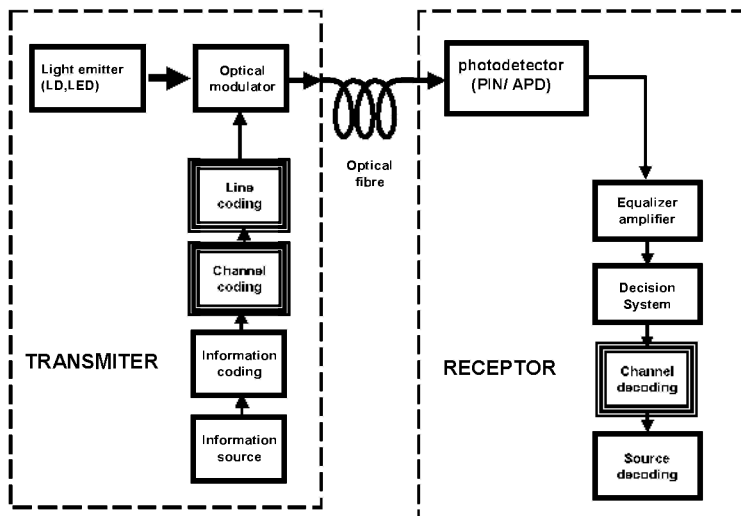


Fig. 1.- Main blocks in a communication system.

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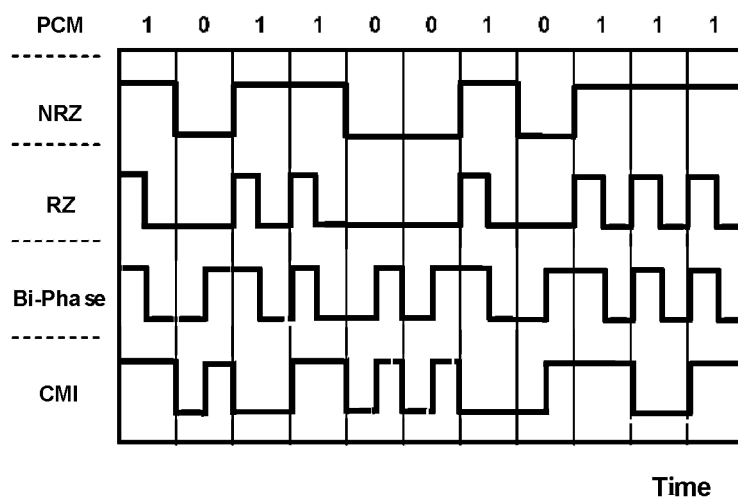


Fig. 2.- Line-coded representations of a pulse-code-modulated signal.

As it was indicated before, three are the basic types of two-level binary codes employed. They are non-return-to-zero (NRZ) format, return-to-zero (RZ) format and the phase-encoded (PE) format. In NRZ codes a transmitted data bit occupies a full bit period. For RZ formats the pulse width is less than a full bit period. In PE format both full-width and half-width data bits may be present. Fig. 2 shows some of the characteristics of the commonly employed codes. A PCM signal appears in four different formats as it can be seen, frequency is double in the last three with respect to the first one. A more general category of codes corresponds to the named "block codes". These binary codes correspond to the $mBnB$ block code class. In this class of codes, blocks of m binary bits are converted to longer blocks of $n > m$ binary bits. These new blocks are then transmitted in NRZ or RZ format. The increase in bandwidth using this scheme is given by the ratio n/m . At the expense of this increased bandwidth, the $mBnB$ block codes provide adequate timing and error monitoring information and they do not have baseline wander problems, since long strings of ones and zeros are eliminated.

2.1. Boolean functions for standard line coding

As it may be appreciated from above indicated concepts, any code has a digital character. This made possible to correlate most common codes with Boolean functions. This is indicated in Table I. It appears, the logic function to be performed with a NRZ signal and reference signal to obtain a particular coding. For instance, if the Boolean function is XOR, Manchester coding is the result. If the function is an AND, the obtained function is an RZ format.

Table I

NRZ		RZ	Manchester Coding	Differential Manchester Coding
Logic Function		AND	XOR	XOR(0), XOR(1)-AND(1)
Data	Reference Signal			
1	10	10	01	01-10
0	10	00	10	10

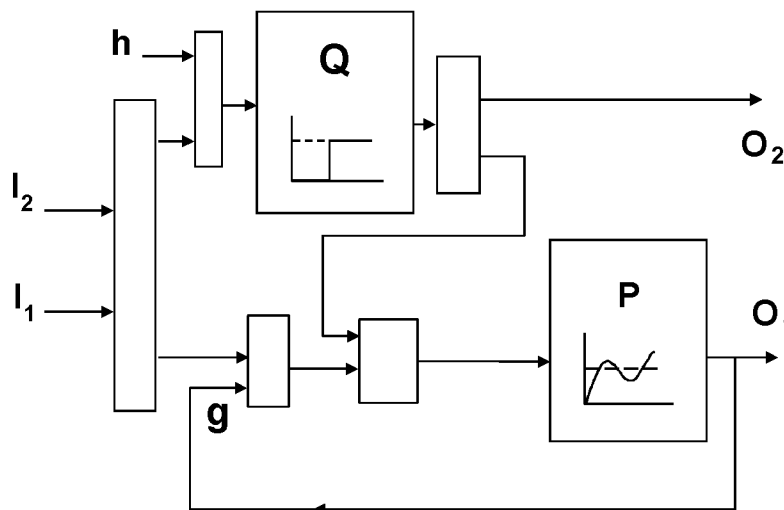


Fig.3.- Optically Programmable Logic Cell main blocks

Moreover, a possible way to implement a structure to implement line coding is, as an Optically Programmable Logic Cell as the one employed by us previously in different architectures for optical computing will show it.

A further point needs to be considered. Any change from a line coding to another requires the presence of another signal. This auxiliary signal, in some aspects it may be considered as a reference clock signal, determines the frequency the final signal will have. It has to be introduced from an external generator. In the case of Table I, this

signal contains two bits in the interval of a previous bit time.

Control signal to P Device

Control signal to Q Device

Table II

	0 – 0.4	0.5 – 0.9	1 – 2
0 – 0.4	XOR	XOR	NAND
0.5	NAND	NOR	NOR
0.6 – 0.9	ON	XNOR	XNOR
1.0	XNOR	XNOR	AND
1.1 – 1.4	XNOR	ON	OR
1.5	AND	OR	OR
1.6 – 2.0	OR	OR	ON
2.0 – 2.5	ON	ON	ON

3. OPTICALLY PROGRAMMABLE LOGIC CELL FOR LINE CODING

3.1. Basic facts of the Logic Programmable Cell

The main block of our coding system is a Logic Programmable Cell employed previously by us as a part of a possible optical computer¹⁻⁴. Although this structure has been reported in several places, some of its principal characteristics will be here presented again. Its main characteristic is the logic processing of two input binary signals, governed by two control signals. Two outputs give logical functions of these inputs. The type of processing is related to the eight main Boolean Functions, namely, AND, OR, XOR, NAND, NOR, XNOR, ON and OFF. The programmable ability of the two outputs, as it has been described, will allow the generation of several data coding for optical transmission. Moreover, as it will be shown too, this circuit has the possibility to the generation of periodic and even chaotic solutions. A precise analysis of the output characteristic versus the main variable parameters, as control signal level and data signal level, has been reported³⁻⁴.

With this configuration, the above-mentioned digital character of the signal is directly obtained. Its main blocks are shown in Fig. 3. Two devices with a non-linear behaviour, P and Q, compose the circuit. The outputs of each one of them correspond to the two final outputs, O_1 and O_2 , of the cell. Four are the possible inputs to the circuit. Two of them are for input data, I_1 e I_2 , and the other two, g and h , for control signals. The way these four inputs are arranged inside the circuit is also represented in Figure 3. A practical implementation we have carried out of the processing element has been based on an optoelectronic configuration. Lines in Fig. 3 represent optical multimode fibres. The indicated blocks, placed in order to combine the corresponding signals, are conventional optical couplers. In this way, optical inputs arriving to the individual devices are multilevel signals. The characteristics of the non-linear devices are also shown in Fig. 3. Device Q, corresponds to a thresholding or switching device, and device P is a multistate device, being the response of this non-linear optical device the one represented in the inbox of Fig. 3. This response is similar to the behaviour of a SEED (Self-Electrooptical Effect Device).

The main aspect concerning above structure is its logic behaviour. Main results appear in Table II. As it can be appreciated, depending on the values given to the control signals, almost any logic function can be obtained. These results will be adopted for the present application

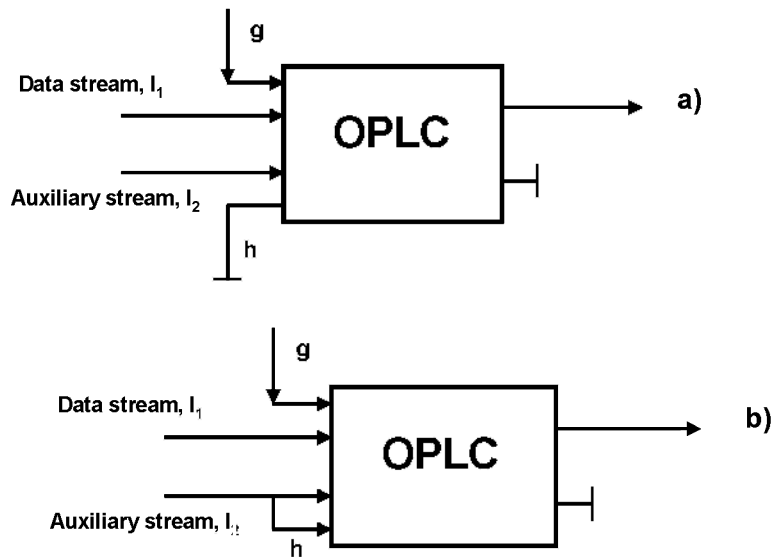


Fig. 4.- Two possible configurations to implement line-coding generators form OPLCs.

Table III

g			h = 0	h = I₂
	I₂	I₁	I₁ + I₂	I₁ + I₂
0 – 0.4	1 0	1	01	01
	1 0	0	11	10
0.5	1 0	1	00	01
	1 0	0	01	01
0.6 – 0.9	1 0	1	10	11
	1 0	0	01	01
1	1 0	1	10	10
	1 0	0	00	01
1.1	1 0	1	11	10
	1 0	0	10	11
1.5	1 0	1	11	10
	1 0	0	11	10
1.6 – 1.9	1 0	1	11	11
	1 0	0	11	10
2	1 0	1	11	11
	1 0	0	11	11

3.2. Possible Codifications

According to Table II the value of the control signals, g and h , impose the logic function to be performed by the cell. Two have been the analyzed situations. They appear in Fig. 4. As it may be seen, control gate g determines the function to be implemented in both cases. Absolute value of the signal there gives rise to a particular logic function. Initial data signal goes through the input designed as Data stream, I_1 . Just one of the output signals works in this configuration. There is one more input signal. It appears in Fig. 4 as “Auxiliary stream, I_2 ”. It corresponds to a periodic signal, composed by alternated “0”s and “1”s bits with a frequency double than the corresponding to the data signal frequency. Control gate h determines, in this case, the type of line coding to be implemented. Two are the analyzed situations. In the first case, situation named as **a)**, this gate has no any signal input applied to it. This has been indicated in he figure as “grounded”. In the second case, situation **b)**, signal input applied to it is the same one than the applied to the second signals input, namely, the auxiliary data stream. The corresponding possible input data appears in Table III. Possible different values for g are given at the left. As it may be seen, they go from 0 to 2. Values for I_1 are the possible input bits, “0” and “1”. In the same way, because the double frequency of the signal going into I_2

and to its periodic characteristics, each possible bit at I_1 correspond with two bits at I_2 , “0” and “1”. The fourth column corresponds to output of the cell when the total input impinging onto the OPLC, according to its internal structure (see Fig. 3) is $I_1 + I_2$. This column corresponds to the **a)** configuration in Fig. 4. As it may be seen, signal output depends strongly on the value given to the control signal.

With these results, the resulting output signals are summarized in Fig. 5. The first row indicates the data signal, composed by “1”s and “0”s with a NRZ code. This stream has to be converted to some other code where timing can be extracted at the receiver. As it was indicated before, this signal is composed with a periodic signal of double frequency. Depending on the values given to the control gate as well as the adopted configuration – **a)** or **b)** – in Fig. 4, the different results appear in the following rows. As it may be seen, several results correspond to some of the previously mentioned binary codes. In this way, for **g** values between 0 and 0.4, and **b)** configuration (Fig. 4), the result corresponds to a Manchester code. If **g** value is between 0.6 and 0.9, **a)** configuration gives a NOT Manchester code. This results appears too for a **g** value of 1 and **b)** configuration. The same value for **g**, but with an **a)** configuration, gives a RZ code. Other values and configurations give similar line codes able to be applied.

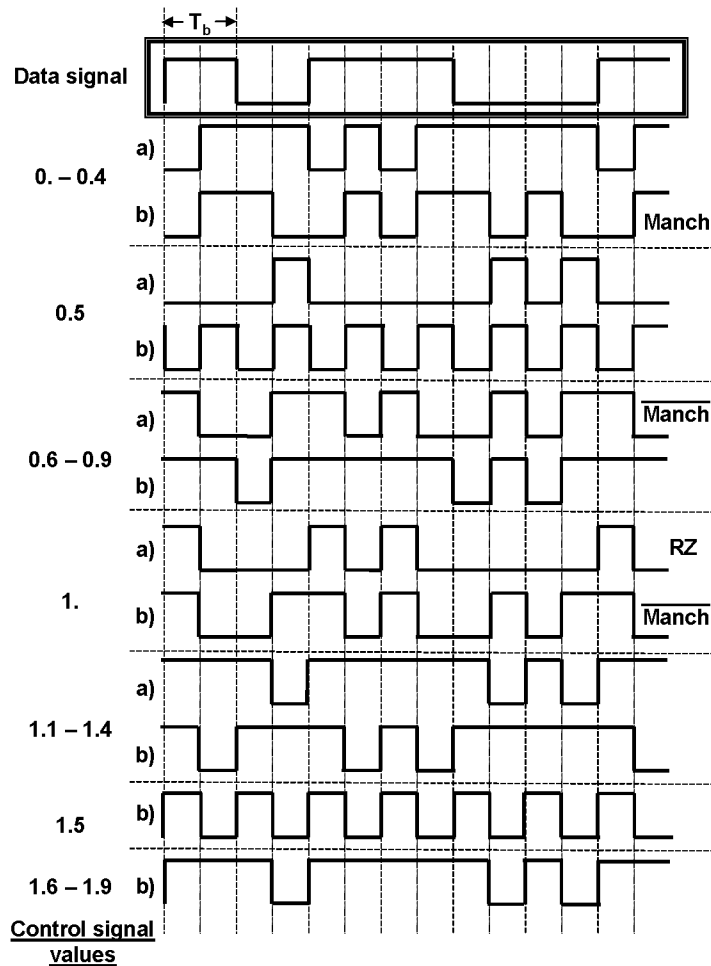


Fig. 5.- Possible Line coding signals according to the value of the control signal. “Manch” corresponds to “Manchester”.

situation, three are the values given to the control signal determining the value of the time delay at the feedback. They are indicated in the figure. As it may be seen, three are the frequencies obtained as output from the OPLC. The first one corresponds to a value of 0.7, the second to 1.5 and the third to 0.3. These results indicate the versatility of our cell as a tool to implement different functions. Moreover, as we have shown in some other places, this cell is able to give chaotic signals and that output may be employed in different applications as encryption or just as pattern generator to analyze a communication systems.

3.3 Optical generator for half-period time auxiliary signal

A possibility given by our OPLC is to obtain an optical generator with a frequency variable able to be applied to different uses. In our present case, the intended application is the obtainment of a periodic signal with a frequency double than the corresponding to the information signal. This periodic signal is needed, as it was shown previously, to obtain the different line codes for a transmission.

The solution to be adopted is to introduce a feedback between an output gate of the OPLC and one of the possible inputs. In our present case we have taken the output corresponding to the P device. This feedback introduces, as it can be seen in Fig. 6, a time delay. This time delay determines the frequency of the oscillation. Moreover, it is necessary to introduce an input signal. In the present case, this signal is a continuous obtained from a step function. It is important to recall that the oscillation frequency is a function of the introduced time delay. This time delay has been designed in such a way that the signal need to set up its configuration, determines the delay and, as a consequence, the frequency. In some way, it works as a VCO (Voltage Controlled Oscillator). The implemented system appears in Fig. 6 where the main blocks are present. Fig. 7 gives an example of its computer simulation. In the present

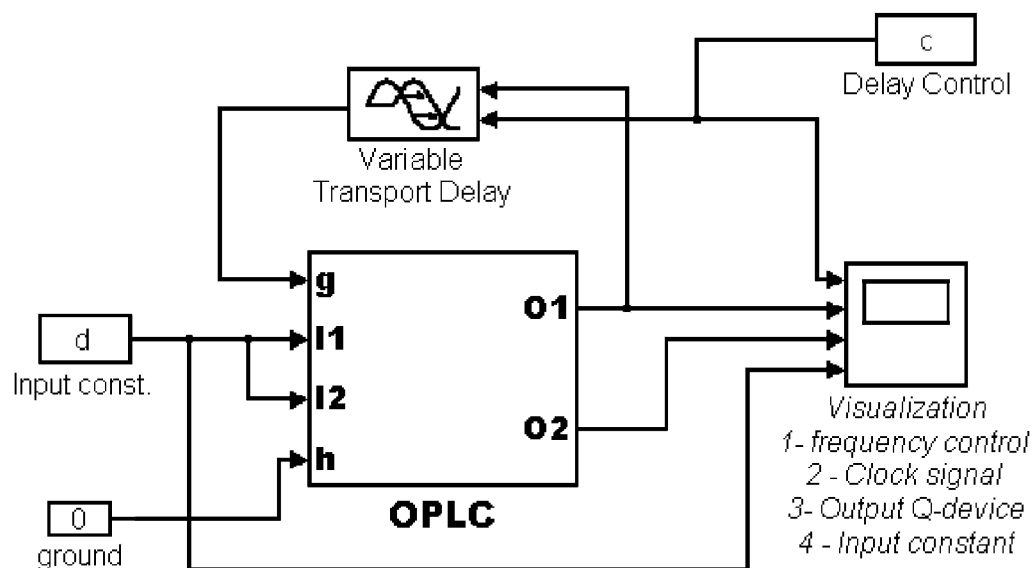


Fig. 6.- Basic configuration of the optical generator for the auxiliary signal.

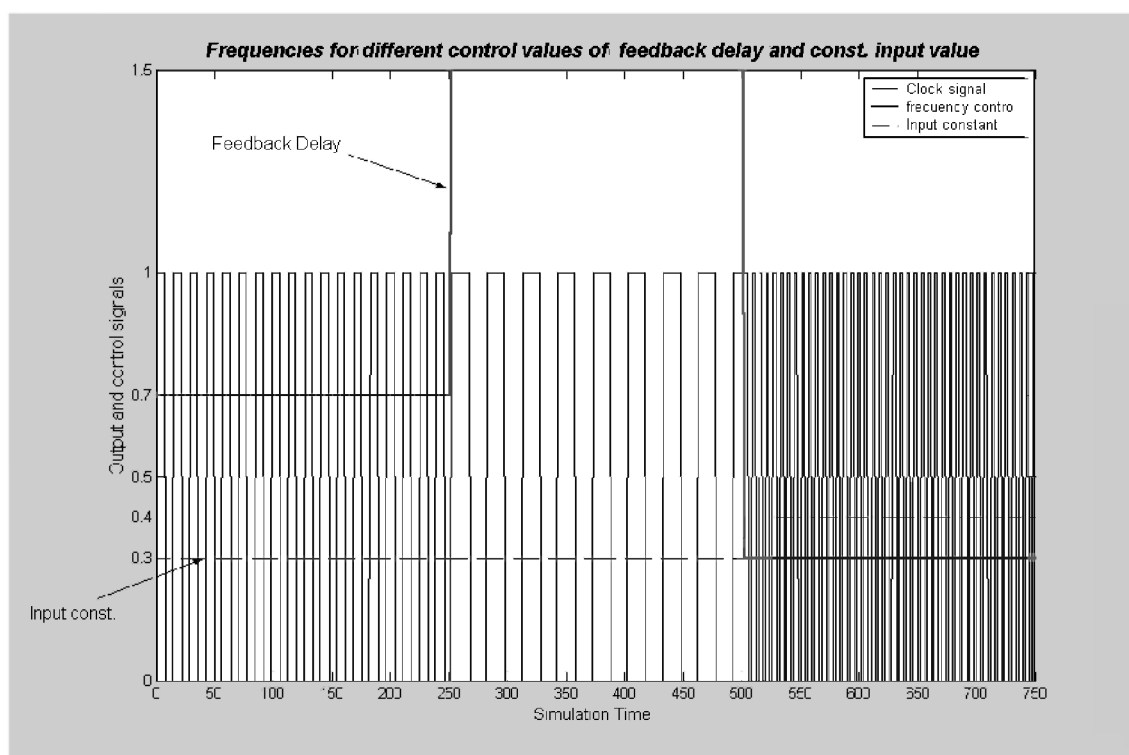


Fig. 7.- Periodic solutions obtained for three different feedback times in Fig. 6.

4. MANCHESTER CODING: EXPERIMENTAL DESIGN

Although the above-described simulation gives a very precise indication about the way an optical programmable logic cell is able to be applied in certain communications topics, we have performed a practical design. The implementation has the intention to show how theoretical concepts may be transferred to a laboratory set up. The design has been performed by optoelectronic methods. It is because that the model we have developed is not a full optical system. Non-linear optical devices, namely P and Q in the OPLC, have been implemented mostly in an electronic way. Optical signals going into the OPLC are converted in electrical signals by a conventional pin photodetector. Optoelectronic circuits are employed where the non-linear behavior appears. The resulting electric signal is finally converted to an optical signal by the corresponding light emitter. This light emitter will be a LED or a LD according to the type of transmission. The experimental set up is shown in Fig. 8. Fig. 8.a shows the practical realization of the OPLC with corresponding input, output and control gates. Fig. 8.b gives the employed electronic circuits. We have performed this electronic implementation because optical non-linear devices, with SEED-like behavior are not commercially available. The behavior of this structure is different with respect to the real one in aspects like processing speed and wavelength dependence. But when one is interested in the characteristics of its possible use, the present structure gives an approximate results.

The experimental obtained results appear in Fig. 9. Lower trace corresponds to the transmitted signal, in this case just a train of “0”s and “1”s in a consecutive sequence (0 1 0 1 ...) Upper trace indicates the signal with a Manchester coding. It is possible to see the way the signal has changes. A “0” bit is converted to a bit time interval where the first half part maintains a zero level and the second half part keeps a “1” level. On the same way, a “1” bit goes to a bit time interval with a higher level at the beginning and zero level in the second part. Peaks indicate beginning and end of bit times. Signal in the middle corresponds to the auxiliary stream with double frequency.

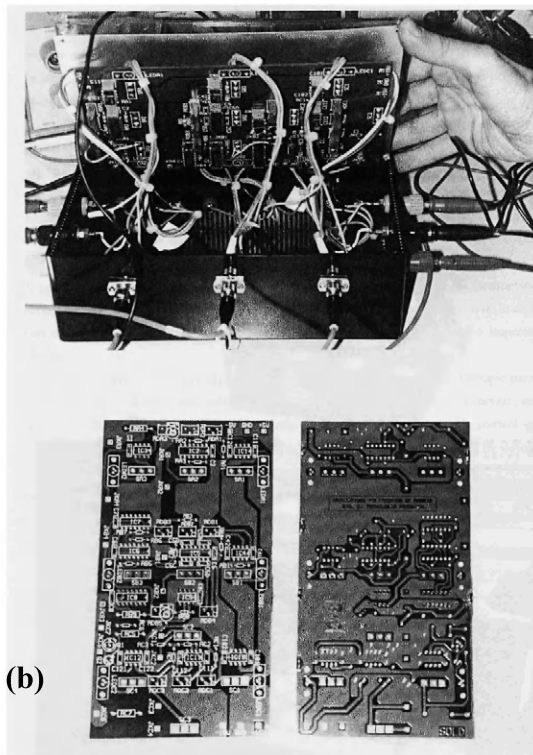


Fig. 8.- Practical realization of the auxiliary signal generator (a) Black box (b) Printed boards.

Above results indicate the correct functioning of the proposed system.

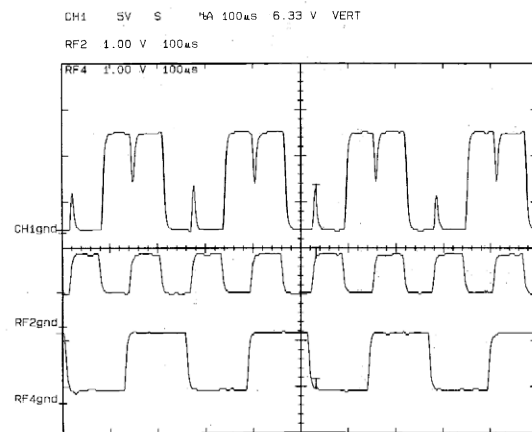


Fig. 9.- Experimental results. Details are given in the text.

5. CONCLUSIONS

The above reported results indicate that optical logic cells are useful tools to implement a large variety of functions in optical communications. Although the origin of these structures was as basic blocks to construct different architectures in optical computing, their possible use in other fields has been proved. The aspects considered in this paper are just a small part of them. As a matter of fact, we have been considering just their use in optical communications links where the distance between emitter and receiver is large. But the use of line coding is not restricted to this area. Namely, small links among different terminals in a small area present similar problems to large distance links. Moreover, the interconnection between different parts in a large computer needs a complex structure of the communications, similar in some aspects to the problems in large areas. This topic needs a more careful analysis.

ACKNOWLEDGMENTS

This work was partly supported by CICYT "Comisión Interministerial de Ciencia y Tecnología", grant TIC99-1131 and CAM "Comunidad Autónoma de Madrid", grant 07T/0037/2000.

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